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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/431,593	11/01/1999	YOSHINORI UEDA	2271/60617	8935

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/431,593	UEDA, YOSHINORI	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 27.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and IDS filed on March 29, 2004.

Allowable Subject Matter

The indicated allowability of claims 1-8 is withdrawn in view of the newly discovered reference(s) to Honna (JP 09-097876 A) submitted with the IDS filed on March 29, 2004. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Honna (JP 09-097876 A) in view of Gardener et al. (US 6,100,173).

In re claim 1, Honna shows (figs. 1 and 2) a semiconductor device comprising a Si substrate, and a resistance element formed on the substrate comprising a plurality of first resistance patterns (31) of polysilicon on the substrate at a first level. The first resistance patterns are arranged in parallel with each other with a mutual separation. A second resistance pattern (41) of diffusion material is provided adjacent to and between the first resistance patterns at a second level lower than the first level. The second resistance patterns are electrically connected in series to the first resistance patterns

(by interconnects 52 and 55) to form the resistance element, wherein the second resistance pattern has an edge defined by the first resistance pattern. Each of the first and second resistance patterns has an identical length (as shown in fig. 2). Each of the second resistance patterns is disposed between a corresponding pair of first resistance patterns such that the first and second resistance patterns are configured in a complementary arrangement in an alternating sequence (abstract). Honna shows all of the elements of the claims except the first and second resistance patterns being a silicide. It is well known in the art that silicide is formed of polysilicon or diffusion regions to form structures having a desired resistance. However, Gardner et al. explicitly discloses (col. 2, lines 12-35) that silicides are formed on gates and diffusion regions to reduce contact resistance and lower the sheet resistance. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the polysilicon resistor and diffusion resistor of Honna by using silicide as taught by Gardner to reduce the contact and sheet resistance of the device.

In re claim 2, Gardener et al. shows (fig. 12) that a resistance element includes an interlayer insulation pattern (14) underneath the first resistance pattern (30) with a shape in conformity with a shape of the first resistance pattern. The second resistance pattern (36) is provided at a level lower that of the interlayer insulation pattern.

In re claim 3, Gardener et al. shows (fig. 12) that the first resistance pattern includes a polysilicon pattern and a polycide region (col. 7, lines 1-24) formed on the polysilicon pattern, the semiconductor device further comprising a MOS transistor (col.

6, lines 15-35) having a polysilicon gate electrode having a composition of the composition of the polysilicon pattern (which is identical).

In re claim 4, neither reference shows that the first and second resistance patterns have the same resistance, however It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resistance patterns having the same resistance, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 5, Gardener et al. discloses (col. 7, lines 25-55) that the second resistance pattern is formed in the Si substrate in the form of a salicide region defined by the first resistance pattern.

In re claim 6, Gardner et al. discloses (col. 6, lines 15-35) that the substrate includes an impurity element with a concentration level such that a parasitic MOS transistor formed of the first resistance pattern acting as a gate electrode and a pair of the second resistance patterns at both sides of the first pattern acting as a source and drain region has a threshold voltage larger than a supply voltage used in the device. Because the device is a MOS transistor, the threshold voltage is large than a supply voltage used in the device.

Allowable Subject Matter

Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
April 18, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800